Amendments to the Specification:

Please delete paragraph [0008] on page 3 of the application and insert in place thereof the following rewritten paragraph:

[0008] The invention is a method and system for generating a synchronous sequence of test vectors from information originating within an asynchronous environment. In a first sequence-generating step, a simulation synchronous sequence of states for functionally verifying proper operations of a simulated integrated circuit (IC) design is provided in a system simulation device (i.e., an IC design tester). The sequence is generated from a simulated asynchronous sequence by extracting a state of the simulated asynchronous sequence at each clock period of a reference clock. Preferably, the reference clock period is equivalent to a tester clock period. Abbreviated system-related delays (which may be "best case" delays encountered within the intended [[in]] system in which the IC is to be integrated) and extended system-related delays (which may be "worst case" delays encountered within the intended system) are preferably considered in this first sequence-generating step.

Please delete paragraph [0042] on page 12 of the application and insert in place thereof the following rewritten paragraph:

[0042] The chip-load timing delay is considered in isolation from any timing delays associated with the system and the tester. The delay should closely approximate the delay of the fabricated chip and is calculated at the chip-level in which every operational delay associated with each internal element (e.g., a transistor or a resistor) is included. Additionally, since different internal elements may be involved in different types of functions (e.g., executing an adding function versus a multiplication function), the time taken to perform one function may vary from the time taken to perform a different function. Thus, the timing delay associated with a first output state may be different from that of [[a]] the next output state. The difference in delay from the first output state to the next output state is the basis for an asynchronous variability among the states.